# CE-ATA Technical Errata

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| **Errata ID** | **Protocol 011** |
| **Affected Spec Ver.** | **Protocol 1.0** |
| **Corrected Spec Ver.** | |

Submission info

| Name | Company | Date |
|---|---|---|
| Amber Huffman | Intel | 08/22/2005 |

Description of the specification technical flaw (add space as needed)

As shown in Figure 12, RW_MULTIPLE_BLOCK (CMD61) Single Block Write Timings, the device may assert MMC Busy after the last MMC data block on a write. This allows the device time to complete the write before accepting a new command from the host.

However, the MMC data layer state machine does not have an allowance for asserting MMC Busy after the last data block on RW_MULTIPLE_BLOCK (CMD61) writes. The only option after the last MMC data block is transferred is to go immediately to idle.

This errata adds a new state that allows the device to assert MMC Busy after the last data block in a RW_MULTIPLE_BLOCK (CMD61) write operation if desired.

Description of the correction

***State DD13: DD_Cmd61W_ChkCnt in section 2.4.2.2.4 shall be modified as shown:***

| DD13: DD_Cmd61W_ChkCnt | Notify ATA layer that MMC data block reception complete. Deliver MMC data block to ATA layer. | | |
|---|---|---|---|
| | 1. Data transmission satisfying the Data Unit Count specified in RW_MULTIPLE_BLOCK (CMD61) not finished and ATA layer not ready to receive more data | → | DD_Cmd61W_Bsy |
| | 2. Data transmission satisfying the Data Unit Count specified in RW_MULTIPLE_BLOCK (CMD61) not finished and ATA layer is ready to receive data | → | DD_Cmd61W_Entry |
| | 3. Data transmission satisfying the Data Unit Count specified in RW_MULTIPLE_BLOCK (CMD61) finished and device does not want to assert MMC Busy | → | DD_Idle |
| | 4. Data transmission satisfying the Data Unit Count specified in RW_MULTIPLE_BLOCK (CMD61) finished and device wants to assert MMC Busy | → | DD_Cmd61W_LastBsy |

***State DD13: DD_Cmd61W_Err shall be modified as shown (refer to ECN 009 for the definition of this state):***

| DD13b: DD_Cmd61W_Err | Notify ATA layer that MMC data block reception was not completed successfully. | | |
|---|---|---|---|
| | 1. Data transmission satisfying the Data Unit Count specified in RW_MULTIPLE_BLOCK (CMD61) not finished and ATA layer not ready to receive more data | → | DD_Cmd61W_Bsy |
| | 2. Data transmission satisfying the Data Unit Count specified in RW_MULTIPLE_BLOCK (CMD61) not finished and ATA layer is ready to receive data | → | DD_Cmd61W_Entry |
| | 3. Data transmission satisfying the Data Unit Count specified in RW_MULTIPLE_BLOCK (CMD61) finished and device does not want to assert MMC Busy | → | DD_Idle |
| | 4. Data transmission satisfying the Data Unit Count specified in RW_MULTIPLE_BLOCK (CMD61) finished and device wants to assert MMC Busy | → | DD_Cmd61W_LastBsy |

***State DD15: DD_Cmd61W_LastBsy shall be added to section 2.4.2.2.4 as shown:***

| DD15: DD_Cmd61W_LastBsy | Assert MMC Busy on DAT0. | | |
|---|---|---|---|
| | 1. ATA layer is ready to receive data | → | DD_Idle |
| | 2. ATA layer is not ready to receive data | → | DD_Cmd61W_LastBsy |

Disposition log

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|---|---|
| 08/22/2005 | Erratum captured |
| 10/14/2005 | Added capability to assert MMC Busy on last data block that has error condition |
| 1/12/2006 | Erratum ratified |